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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

| EXAMINER | |
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| PETRANEK, JACOB ANDREW | |

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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/530,495
Filing Date: April 06, 2005
Appellant(s): SETHURAMAN ET AL.

Aaron Waxler; Reg. No. 48,027
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 8/20/2009 appealing from the Office action mailed 9/24/2008.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

Fisher et al. (U.S. 6,026, 479), Jensen et al. (U.S. 7,149,878), Lilja et al. ("Exploiting the parallelism available in loops," IEEE, pages 13-26, February 1994),

Sanches et al. (U.S. 2002/0116596), and Maiyuran et al. (U.S. 2002/0129201) are relied upon as evidence.

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Maintained Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7, and 15-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878).

3. As per claim 1:

Fisher discloses a data processing apparatus the apparatus comprising:

an instruction memory address generation circuit for outputting an instruction address (Fisher: Figure 2 elements 120 and 122, column 5 lines 54-61)(The cache memory is inherently addressed by a program counter that generates an instruction address.);

an instruction memory system arranged to output an instruction word addressed by the instruction address (Fisher: Figure 2 elements 120 and 122, column 5 lines 54-61)(The caches are a subset of the instruction memory system, which obvious to one of ordinary skill in the art also include main memory and disk memory. They inherently

output instructions by instruction addresses generated by a program counter.), including at least one type of memory selected to achieve a desired instruction cycle time (Fisher: Figure 6 elements 620 and 622, column 8 lines 48-60)(The memory is selected to be a cache to achieve faster performance and access to the instructions.) wherein longer instruction words are stored in said memory system within memory ranges of progressively shorter instruction words associated with

a corresponding memory type (Fisher: Figure 6 element 620 and 622, column 8 lines 41-65)(The high and low ILP instructions are stored within ranges stored in the instruction cache.);

an instruction execution unit, arranged to process a plurality of instruction from the instruction word in parallel (Fisher: Figure 2 elements 150A-D, column 5 lines 26-37)(The execution units process instructions in parallel for high ILP code.).

Fisher failed to teach a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies, the detection unit being coupled to the instruction execution unit that parallelizes processing of the instructions from the instruction word, dependent on a detected range.

However, Jensen disclosed a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies, the detection unit being coupled to the instruction execution unit that parallelizes processing of the instructions from the instruction word, dependent on a detected range (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines

1-25)(The combination uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

The advantage of mode switching through detecting a range of addresses over Fisher's methods is that it allows for eliminating mode switching instructions and reducing time consuming interrupts to switch modes (Jensen: Column 3 lines 48-67 continued to column 4 lines 1-9)(Fisher: Column 6 lines 26-47). One of ordinary skill in the art would have been motivated by this advantage to implement the mode switching method of Jensen into the processor of Fisher. Thus, one of ordinary skill in the art would have been motivated by the advantages of reducing the program size and limiting the number of required interrupts to implement the method of mode switching of Jensen into the processor of Fisher.

4. As per claim 2:

Fisher and Jensen disclosed a data processing apparatus according to claim 1, wherein the instruction execution unit and/or the instruction memory system is arranged to adjust a width of the instruction word that determines a number of instruction from the instruction word that is processed in parallel (Fisher: Figure 2 elements 150A-D, column 5 lines 26-37 and column 6 lines 37-47)(The execution units execute full VLIW instructions or partial VLIW instruction dependent on the mode of the processor.), dependent on the detected range (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

5. As per claim 3:

Fisher and Jensen disclosed a data processing apparatus according to claim 1, wherein the instruction execution unit comprises a plurality of functional units (Fisher: Figure 2 elements 150A-D, column 5 lines 26-37), the instruction execution unit being arranged to select a subset of the functional unit that is available for processing the instructions (Fisher: Figure 2 element 150D, column 6 lines 55-63)(The low ILP mode uses a subset of the function units available for processing.), dependent on the detected range (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

6. As per claim 4:

Fisher and Jensen disclosed a data processing apparatus according to claim 1, wherein the instruction execution unit comprises a plurality of functional units (Fisher: Figure 2 elements 150A-D, column 5 lines 26-37), the instruction execution unit being arranged to select whether functional units or groups of functional unit from a set of functional unit each receive respective instructions from the instruction word, or receive a shared instruction from the instruction word (Fisher: Figures 2-3, column 5 lines 62-67 continued to column 6 lines 1-25)(An individual functional unit is used in low ILP mode and the entire execution unit is used in high ILP mode.), dependent on the detected range (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination uses Jensen's method

of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

7. As per claim 5:

Fisher and Jensen disclosed a data processing apparatus according to claim 1, wherein the instruction memory comprises a first memory unit and a second memory unit (Fisher: Figure 2 element 120 and 122, column 5 lines 54-61), providing storage with a first and second unit of width of addressable memory locations for instruction words of different lengths with addresses in a first and second range respectively, the first and second unit of width being mutually different (Fisher: Column 7 Line 15-26)(The low ILP and high ILP modes use different VLIW instruction lengths. The different instruction lengths are inherently located at different addressable memory location widths.).

8. As per claim 7:

Fisher and Jensen disclosed a data processing apparatus according to claim 5, comprising a memory mapping unit arranged to map the instruction address onto the first memory unit of the second memory unit, dependent on the detected range (Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The instructions are mapped to the main cache or the mini cache dependent on the range of the instruction being in a high ILP process or being in a low ILP process.).

9. As per claim 15:

Claim 15 essentially recites the same limitations of claim 1. Therefore, claim 15 is rejected for the same reasons as claim 1.

10. As per claim 16:

The additional limitation(s) of claim 16 basically recite the additional limitation(s) of claim 2. Therefore, claim 16 is rejected for the same reason(s) as claim 2.

11. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 3. Therefore, claim 17 is rejected for the same reason(s) as claim 3.

12. Claims 6 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878), further in view of Lilja et al. ("Exploiting the parallelism available in loops," IEEE, pages 13-26, February 1994).

13. As per claim 6:

Fisher and Jensen disclosed a data processing apparatus according to claim 5, programmed to execute a program, longer instruction words being stored in the first memory unit (Fisher: Figure 2 element 120, column 5 lines 62-67 continued to column 6 lines 1-7)(The high ILP instructions are longer in length than the low ILP instructions.), shorter instruction words being stored in the second memory unit (Fisher: Figure 2 element 120, column 6 lines 8-25)(The low ILP instructions are shorter in length than the high ILP instructions), the first unit of width being larger than the second unit of width (Fisher: Figure 2 elements 120 and 122, column 5 lines 62-67 continued to column 6 lines 1-25)(The high ILP instructions are wider instructions because they contain 4 operations compared to the single operation in low ILP instructions.).

Fisher and Jensen failed to teach longer instructions words coming from an inner loop and shorter instruction words from a majority of the program outside the inner loop.

However, Lilja disclosed longer instructions words coming from an inner loop and shorter instruction words from a majority of the program outside the inner loop (Lilja: Page 13 lines 15-16)(Lilja disclosed that loops contain a larger amount of parallelism. Thus, it's obvious to one of ordinary skill in the art that the high ILP instructions are from loops and low ILP instructions are outside of loops.)

Lilja disclosed that most of the parallelism of a program is contained within loops (Lilja: Page 13 lines 15-16). One of ordinary skill in the art would have been motivated by this to put high ILP instructions from a loop into the main cache and low ILP instructions outside of a loop into the mini cache of Fisher. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement placing high ILP instructions coming from a loop and low ILP instructions coming from outside of loops into their respective caches because of the fact that most parallelism occurs within loops.

14. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 6. Therefore, claim 14 is rejected for the same reason(s) as claim 6.

15. Claims 8-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878), further in view of Maiyuran et al. (U.S. 2002/0129201).

16. As per claim 8:

Fisher and Jensen disclosed a data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable the first memory unit when addresses in the second range are detected (Fisher: Column 7 lines 15-37 and column 8 lines 21-25)(Fisher disclosed deactivating the mini cache when instructions are being fetched from the main cache.).

Fisher and Jensen failed to teach disable supply of clock signals to the first memory.

However, Maiyuran disclosed disable supply of clock signals to the first memory (Maiyuran: Paragraph 28)(A cache is disabled by using clock signals.).

Fisher disclosed that caches can be deactivated when they are not being used to fetch instructions from, but didn't detail how the caches are actually deactivated. One of ordinary skill in the art would have been motivated by this lack of information to find Maiyuran that disclosed that caches can be disabled by using clock signals. Thus, it's obvious to one of ordinary skill in the art to implement the use of clock signals to disable the caches of Fisher when they aren't in use.

17. As per claim 9:

Fisher and Jensen disclosed a data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable all but the memory unit from whose address range addresses are detected (Fisher: Column 7 lines 15-37 and column 8 lines 21-25)(Fisher disclosed deactivating the mini cache when instructions are being fetched from the main cache.).

Fisher and Jensen failed to teach disable supply of clock signals to the first memory.

However, Maiyuran disclosed disable supply of clock signals to the first memory (Maiyuran: Paragraph 28)(A cache is disabled by using clock signals.).

Fisher disclosed that caches can be deactivated when they are not being used to fetch instructions from, but didn't detail how the caches are actually deactivated. One of ordinary skill in the art would have been motivated by this lack of information to find Maiyuran that disclosed that caches can be disabled by using clock signals. Thus, it's obvious to one of ordinary skill in the art to implement the use of clock signals to disable the caches of Fisher when they aren't in use.

18. Claims 10 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878), further in view of Sanches et al. (U.S. 2002/0116596).

19. As per claim 10:

Fisher and Jensen disclosed a data processing apparatus according to claim 2, wherein the instruction memory system comprises a plurality of memory units (Fisher: Figure 2 element 120 and 122, column 5 lines 54-61), each arranged to be responsive to instruction addresses in a respective range (Fisher: Figure 2 element 120 and 122, column 5 lines 54-61)(Jensen: Figure 4, column 13 lines 7-22)(Each memory stores a range of addresses.), the instruction memory system being arranged to supply the instruction word as a combination of instructions from those of the memory units in

whose respective range the instruction address lies (Fisher: Figure 2 element 120, column 5 lines 27-37)(The high ILP instruction word is a combination of instructions that are stored in the main cache based on its instructions address.).

Fisher and Jensen failed to teach the instruction memory allowing partial overlap of the respective ranges.

However, Sanches disclosed the instruction memory allowing partial overlap of the respective ranges (Sanches: Paragraph 42)(Sanches allows for sequential in order program instructions to be stored in different memory banks.).

The advantage of the system of Sanches is that it allows for avoiding the storing of VLIW instructions that contain nop instructions (Sanches: Paragraph 15). The advantage of not using as many nop instructions in VLIW instructions is that the code size of the overall program is reduced. One of ordinary skill in the art would have been motivated by this advantage to implement the memory system of Sanches in Fisher. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the memory system of Sanches in Fisher for the advantage of reducing the storing of nop instructions.

20. As per claim 12:

Fisher, Jensen, and Sanches disclosed a data processing apparatus according to claim 10, wherein the execution unit comprises groups of one or more functional units (Fisher: Figure 2 elements 150A-D), each group being coupled to a respective predetermined one of the memory units, for receiving instructions from the instruction words (Fisher: Figure 2 elements 120 and 150A-D), when the instruction address is in

the respective range of the respective predetermined one of the memory unit to which the group is coupled (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

21. Claim 11 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878), further in view of Sanches et al. (U.S. 2002/0116596), further in view of Maiyuran et al. (U.S. 2002/0129201).

22. As per claim 11:

The additional limitation(s) of claim 11 basically recite the additional limitation(s) of claim 8. Therefore, claim 11 is rejected for the same reason(s) as claim 8.

**(10) Response to Argument**

23. Regarding claims 1-5, 7, and 15-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878):

A.) Appellant argues "However, contrary to the assertions made by the Examiner in rejecting the claims, neither Fisher nor Jensen teach or suggest the ordering of longer instructions contained within ranges of progressively shorter

instructions and that the association of memory type for storing the instructions, as is recited in the claims."

The examiner disagrees for the following reasons. The limitation in question is "wherein longer instruction words are stored in said memory system within memory ranges of progressively shorter instruction words associated with a corresponding memory type." Thus, in order to read on the limitation, the high ILP instructions (i.e. longer instruction words) of Fisher must be stored within a memory range that also stores low ILP instructions (i.e. shorter instruction words) of the memory system. Since there is no explicit memory range recited, there are a number of ways that Fisher inherently reads upon the claimed limitation. If the memory range is inclusive of the entire hard drive or disk, which is part of the memory system, then Fisher inherently stores both high and low ILP instructions within that range on the disk. This is inherent looking at the instruction caches of Fisher in figure 6 because all instructions cached in the processor inherently originate from a non-volatile disk or hard drive. Thus, a memory range incorporating all addressable memory space within a processor inherently reads upon the claimed limitation because the disk inherently stores both high and low ILP instructions.

Additionally, when the memory range is a smaller range that encompasses the entire memory space of a process, high and low ILP instruction are inherently in the memory range. One of ordinary skill in the art at the time of the invention is well aware that a process defines a program that is to be executed on a processor. A process additionally includes the address space that all instructions and all data used by the

program are stored in, i.e. the memory range that is to be used by the process. Since the processor of Fisher inherently executes processes that can include both high and low ILP instructions, Fisher inherently discloses that high and low ILP instructions are within a memory range that is equal to the memory range of the process that the high and low ILP instructions are a part of.

Finally, the memory range in Fisher can be as small as four instructions and still read on the claimed limitation, where the four instructions include a transition between switching from high to low ILP instructions, or vice versa. Thus, this memory range would include a couple instructions from both the high and low ILP instructions. Therefore, the high ILP instructions are stored within a memory range of the low ILP instructions. In fact, Jensen disclosed a great illustration that is obvious to one of ordinary skill in the art as to how instructions can be ordered and where a transition would occur. Jensen shows in figure 4 element 410 that instructions in program order transition into different ISA's at different physical addresses of a memory range. A transition from the last few instructions of element 419 into the first few instructions of element 418 shows how a memory range as small as four instructions can still read upon the claimed limitation.

Thus, each of these three examples shows how Fisher disclosed the claimed limitation of storing longer instruction words (i.e. high ILP instructions) within a memory range of shorter instruction words (i.e. low ILP instructions).

B.) Appellant argues "Hence, Fisher fails to provide any teaching regarding switching between one memory or another based on a memory address range and

specifically refers to a controller to determine whether one memory or the other is to be accessed. This assess is based on the length of the instruction and not the memory address of the instruction."

In response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., switching from one memory to another based on a memory address range) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Even if this limitation were indeed claimed, Fisher clearly teaches it. Fisher stores low and high ILP instructions in different instruction caches, elements 122 and 120 respectively. When fetching is changed from one instruction cache to another via a switch instruction or interrupt (column 6 lines 26-47), inherently the fetching in the newly selected cache is in a different memory range than the previously fetched instructions in the previously selected cache because the first memory range can be defined from instructions from low/high ILP instructions and the instructions from the second memory range can be defined from high/low ILP instructions.

Finally, if the appellant was referring to the claimed "detection unit" limitation, this limitation is taught by the combination of Fisher and Jensen.

C.) Appellant argues "However, the incorporation of the teaching of Jensen into that of Fisher would render the device disclosed by Fisher unsuitable for its intended purpose. Fisher discloses an instruction level controller that causes a switch

between a main memory and a mini-instruction memory. The instruction level controller receives an interrupt to determine whether to access the main cache memory or the min-instruction memory. (see for example, col. 6, lines 7-13 "[t]he instruction level controller 140 switches to a low ILP mode upon receiving a LOW ILP mode signal, such as an interrupt, a procedure call instruction designated as a low ILP call, or a predetermined 'gateway' instruction executed by the CPU 100.")."

The examiner disagrees for the following reason. The appellant has not attempted to define what Fisher's intended purpose is in the argument nor does the appellant explain how the modification renders the intended purpose unsuitable. The examiner would argue that the intended purpose of Fisher is to segregate high and low ILP instructions in different caches and enable a mode to select which cache to fetch instructions from. Fisher disclosed that switching from fetching high to low ILP instructions, or vice versa, is accomplished by either a switching instruction or an interrupt. Both methods have their disadvantages since both are using a software solution for switching modes. The disadvantage of using a switch instruction is that it adds additional instructions into the program, which causes the program size and program execution time to increase. The disadvantage of using an interrupt is that performance is hurt by the operating system call needed to handle an interrupt to change the fetch mode. The modification with Jensen uses a hardware solution that is capable of switching modes based on detecting a change in memory ranges. Thus, Jensen's solution doesn't have the disadvantages of Fisher's solutions and has the advantage of reducing program code and increasing performance over both of Fisher's

solutions. Thus, the combination, with proper motivation, doesn't render Fisher unsuitable for its intended purpose.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jacob Petranek/

/JAP/

November 17, 2009

Conferees:

Eddie Chan

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183

Kevin Ellis
/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117